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(54) **A modulator, in particular a sigma-delta modulator.**

(57) A high-order sigma-delta modulator comprises at least two integrator stages (H1-Hn). The first one, two or three integrator stages (H1-H3) of the high-order modulator form a low-order modulator which is stable at all input signal values. The arrangement comprises a means (31) for resetting those integrator stages (H3-Hn) subsequent to the low-order modulator when the stable operation input signal range of the high-order modulator is exceeded. Thus, in the stable operation range, the modulator operates as a high-order modulator, whereas outside this range, the modulator operates as a low-order modulator and so operates stably at all input signal amplitudes.

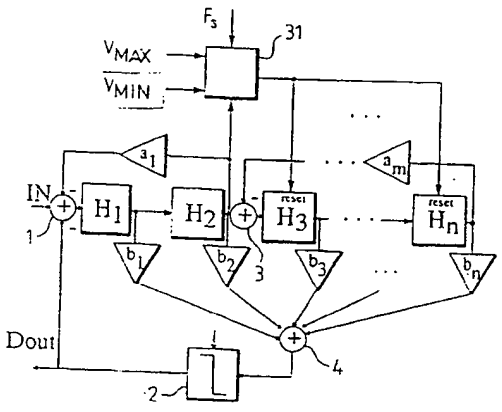

FIG. 3

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The invention relates to a modulator, in particular a high-order sigma-delta modulator comprising at least two integrator stages.

The need for high-resolution analog-to-digital (A/D) converters has increased the use of noise shaping techniques based on oversampling and sigma-delta modulation. The resolution of a sigma-delta A/D modulator is determined by the oversampling ratio (M) and the order of the noise shaping function. There are, however, severe stability problems associated with high-order (≧2) sigma-delta modulators.

The stability of high-order modulators is dependent on the amplitude of an incoming signal. When the modulator assumes an unstable mode of operation, the voltages of its integrators increase abruptly, and the bit stream from the output of the modulator begins to oscillate independently of the input signal. The high-order modulator does not return to the linear operation range even though the input would return to the stable operation range. In known solutions to the problem, the modulator is maintained stable by resetting all integrators during excessive input signal values or by accurately limiting the voltage range of the integrators within the stable operation range.

The problem with the limiting of the voltage range of the integrators is the technical realization. Above all, it is necessary to avoid any unnecessary circuits in the first stages of the modulators, in which the sensitivity of the modulator is at its highest. With a signal-to-noise ratio exceeding 16 bits (98 dB), the required circuits are difficult to effect. The sensitivity of the modulator to interferences decreases rapidly in the subsequent integrator stages, and therefore it is advisable to make the additional circuits in these stages.

In addition, the resetting of all integrators in a multiple-feedback (MF) type modulator causes a reduction in the power of the bit stream from the modulator output when input signal levels are above the stable operation range. As a result of this, values obtained from a decimalization filter following the modulator are smaller than within the normal operation range. This is very detrimental in practical applications. It is normally desired that the output is saturated to a maximum value when the amplitude of the input signal exceeds its operation range. In a feedforward (FF) type modulator the resetting of the integrator stages can be used without the problems described above.

As is well-known, a low-order i.e. a first-order modulator is stable irrespective of the level of the input signal and so is a second-order sigma-delta modulator. A third order modulator can be made stable in practical applications by limiting the integrators to a stable operation range by the operating voltages. Modulators of a higher order than that require external stabilization. The conventional resetting of all integrators for stabilizing the modulators causes interference in the signal.

According to the present invention, there is provided a modulator, comprising at least two integrators coupled together in series and arranged to receive an input signal characterised by means for lowering the order of the modulator when the amplitude of the input signal exceeds the range at which the modulator will operate stably. This has the advantage that such resetting is avoided. Thus, stability is ensured, and the resetting of the first integrator stage or the first integrator stages is avoided by lowering the order of the high-order modulator so as to convert the modulator temporarily into a first-, second-, or third-order modulator, which is stable irrespective of the level of the input signal, when the level of the input signal exceeds the stable operation range of the high-order modulator, which is detected by monitoring the voltages of the integrator stages. When the level of the input signal is within said stable operation range, the modulator operates in a normal way as a high-order modulator, and so the better quantization noise shaping properties of the high-order modulator are obtained.

The invention will now be described, by way of example only with reference to the accompanying drawings, of which:

Figures 1 and 2 show block diagrams of prior art sigma-delta modulators realized in a feedforward (FF) configuration and a multiple feedback (MF) configuration, respectively;

Figure 3 shows a block diagram of an FF-type sigma-delta modulator, in which the stabilization according to the invention is applied;

Figure 4 shows a block diagram of an FF-type sigma-delta modulator, in which the stabilization according to the invention is applied; and

Figures 5, 6 and 7 are graphic representations of the digital output Dout of the modulators of Figures 1, 2 and 4, respectively, as a function of an input signal IN.

Sigma-delta modulators can be realized by using either a feedforward (FF) configuration, as in Figure 1, or a multiple feedback (MF) configuration, as in Figure 2. The sigma-delta modulators in Figure 1 and Figure 2 comprise a series connection of n integrator stages H1, H2, ... Hn, where n is a positive integer. The order of the modulator is equal to the number of the integrator stages. A modulator comprising at least two integrator stages (a second-order modulator) is called a high-order modulator. In the following these two well-known modulator structures will be described generally.

In the FF-type modulator shown in Figure 1, an output signal Dout of a quantizer 2 (and of the entire modulator) and an output voltage of the second integrator H2 scaled by a feedback coefficient a1 are subtracted from an input signal IN of the modulator in a subtractor means 1. The output of the subtractor means 1 is applied to the first integrator stage H1 having an output connected to the second integrator stage H2. An output voltage of the last integrator

stage Hn is scaled by a feedback coefficient am and then subtracted from the output of the second integrator stage H2 in a subtractor means 3, and the difference is applied to the third integrator stage H3. The output voltage of each integrator stage H1 ... Hn is scaled with a respective weighting coefficient b1 ... bn and applied to a summing means 4 having an output connected to the quantizer or comparator 2. The quantizer 2, the subtractor means 1 and 3, the summing means 4 and the transfer of the integrator voltages from one integrator stage to a subsequent one is controlled by an oversampling clock Fs.

In the MF-type modulator shown in Figure 2 a digital output signal Dout of a quantizer 22 (and of the entire modulator) is scaled by a feedback coefficient bn and subtracted from an input signal IN of the modulator in a subtractor means 21_n and then applied to the first integrator stage Hn. A similar subtractor means 21_{n-1} ... 21_1 is provided in the input of each subsequent integrator stage H_{n-1} ... H_1 for subtracting an output signal Dout scaled by a respective feedback coefficient b_{n-1} ... b_1 from the output signal of a preceding integrator and applying the difference to the input of a subsequent integrator stage. The subtractor means 21_n also subtracts the output voltage of the integrator stage H_3 scaled by a feedback coefficient a_m from the input signal IN. Correspondingly, the subtractor 21_2 also subtracts the output voltage of the last integrator stage H1 scaled by a feedback coefficient a_1 from the output signal of the integrator stage H3. The quantizer 22 and the subtractor means 21_n ... 21_1 are controlled by the oversampling clock Fs. The feedbacks a_1 ... a_m are not necessary in the modulator. The quantization noise can be shaped by these coefficients so that the amount of noise on the pass band decreases as compared with a modulator without such feedback coefficients.

As to the practical applications of modulators, reference is made to the doctoral thesis *High Performance Analog Interfaces for Digital Signal Processors*, Frank OP 'T Eyende, Katholieke Universiteit Leuve'n, November 1990, and the article *Design of stable high order 1-bit sigma-delta modulators*, Tapani Ritoniemi et al., Proceedings of IEEE International Symbosium on Circuits and Systems, May 1990, pp. 3267-3270, which describes the design of third-, fourth-, fifth-, and sixth-order FF and MF modulators when using the Switched capacitor (SC) technique. The article also describes stability problems and solving such problems by limiting the input signal.

As already mentioned above, another prior art technique for stabilizing a sigma-delta modulator is to reset all modulator integrator stages.

Figures 5 and 6 show the digital outputs Dout of the fifth-order modulators of Figures 1 and 2 as a function of the input signals IN. The stable linear range of the modulator extends up to a point A. When the input level IN exceeds the point A, all modulator integrator stages are reset to return the modulator from the unstable mode. In Figure 5 the output Dout of the FF modulator is thereby saturated to a value equal to or greater than its maximum value, which is the desired result. In Figure 6, the resetting of the integrators of the MF modulator causes a reduction in the power of the outbound bit stream on signal levels above the point A, and so values obtained from the decimalization filter following the modulator are smaller than within the normal stable operation range of the input signal. This phenomenon is very detrimental in practical applications.

The invention aims at improving the stability of a high-order modulator when the amplitude of the input signal exceeds its normal stable operation range by temporarily lowering the order of the high-order modulator so that it is stable irrespective of the amplitude of the input signal of the modulator. In the preferred embodiment of the invention, the output voltage of the first, second or third integrator of the modulator is monitored and the order of the modulator is lowered by resetting all integrators following the integrator which is being monitored when the output voltage of the integrator being monitored exceeds a predetermined threshold value.

In the following this basic idea of the invention will be described by means of two illustrating embodiments.

The block diagram of Figure 3 illustrates the realization of the stabilization according to the invention in a sigma-delta modulator of the feedforward (FF) type shown in Figure 1. The structure of the sigma-delta modulator itself is substantially similar to that of Figure 1, wherefore only differences relevant to the invention will be described below. The same reference numerals and symbols in Figures 1 and 3 indicate the same items or functions.

In the embodiment of Figure 3, the first two integrator stages of the high-order (n-order) sigma-delta modulator form a second-order sigma-delta modulator which is stable irrespective of the level of the input signal IN. The stabilization circuit comprises a comparator means 31 to one input of which the output voltage of the second integrator stage H2 (i.e. of said second-order modulator) is connected. In addition, two reference voltages Vmax and Vmin representing the highest and lowest value of the stable range of the input voltage IN are connected to the comparator circuit 31. The output of the comparator circuit 31 is connected to resetting inputs RESET in the integrator stages H3 ... Hn following the integrator stage H2 being monitored. When the input signal IN is within said stable linear range, the modulator of Figure 3 operates in a normal way as an n-order modulator. When the comparator circuit 31 detects that the output voltage of the integrator stage H2 exceeds the reference voltage Vmax, the state of the output of the comparator

circuit 31 is changed, as a result of which the integrator stages H3 ... Hn are reset and only the first two integrator stages H1 and H2 remain in operation, thus forming the modulator output Dout through the summing means 4 and the quantizer 2. In this way the n-order modulator of Figure 3 is temporarily converted into a second-order modulator, which is stable at all values of the input signal. Accordingly, the output signal at the modulator output Dout is stable, though also relatively noisy, even at input signal values outside of the stable operation range of the n-order modulator. The comparator means 31 maintains the integrator stages H3 ... Hn reset until the output voltage of the integrator stage H2 is again smaller than Vmax, that is, the input signal IN has returned to the stable operation range. Above, the output voltage of the integrator stage H2 is monitored. Alternatively, it is also possible that only the first integrator stage H2 is made stable and its output voltage is monitored, or a modulator comprising the first, second and third integrator stages H1, H2 and H3 is made stable at all values of the input signal IN and the output voltage of the integrator stage H3 is monitored. Also in this case, all integrator stages following the integrator stage being monitored are reset.

Figure 4 shows another embodiment of the invention, in which the stabilization according to the invention is applied in a sigma-delta modulator of the multiple feedback (MF) type shown in Figure 2. The modulator arrangement itself is substantially similar to that shown in Figure 2, and only differences relevant to the invention will be described below. The same reference numerals in Figures 2 and 4 indicate the same items or functions. In the embodiment of Figure 4, the first, the first two, or the first three integrator stages Hn, Hn-1 and Hn-2 form a first-, second-, or third-order sigma-delta modulator, respectively, which is stable irrespective of the amplitude of the input signal IN. The output of this first-, second-, or third-order modulator is connected to a first input IN1 in a selector means or an analog multiplexer 41. The output of the last integrator stage H1 in the n-order modulator is connected to a second input IN2 in the multiplexer 41. The output of the multiplexer 41 is connected to the quantizer 22. The multiplexer 41 couples either one of its inputs IN1 and IN2 to the quantizer 22, depending on the state of a selection signal SEL. The output voltage of the last integrator H1 of the n-order modulator is connected to one input in a comparator circuit 42. Reference voltages Vmax and Vmin representing the upper and lower limits of the stable range of the input signal IN and an oversampling clock signal Fs synchronizing the comparator circuit with the operation of the rest of the modulator are also connected to the comparator circuit 42. The output of the comparator circuit 42 is connected to the resetting input RESET of the integrator stages H3, H2 and H1 following said low-order modulator, to a setting input SET of an RS flip-flop and to the input of a delay means 44. The output of the delay means 44 is connected to a resetting input RESET of the RS flip-flop 43. A non-inverted output Q of the RS flip-flop 43 generates the selection signal SEL for the multiplexer 41. When the input signal IN is within its stable operation range, the connection of Figure 4 operates as an n-order modulator, and so the multiplexer 41 couples the input IN2 to the quantizer 22. When the comparator means 42 detects that the output voltage of the integrator stage H1 exceeds the reference voltage Vmax, the state of the output of the comparator means 42 is changed so that the integrator stages H3, H2 and H1 are reset and the state of the output of the RS flip-flop 43 is changed. As a result, the multiplexer 41 couples the input IN1 to the quantizer 22. According to the invention, the modulator of Figure 4 thereby acts as a first-, second-, or third-order modulator, which is stable irrespective of the level of the input signal IN. This is continued until the output voltage of the integrator stage H1 is again smaller than the reference voltage Vmax. The state of the comparator means 42 is then changed so that the integrator stages H3, H2 and H1 are released. The multiplexer 41, however, maintains the input IN connected to the quantizer 22 during the delay of the delay means 44, which is at least equal to the delay of the integrator stages H3, H2 and H1 following the low-order modulator (at least one clock cycle per each delaying integrator stage). Delaying is required in order that the signal would have time to propagate to the last integrator H1 before its output is again selected as the input of the quantizer 22.

Figure 7 shows the output Dout of the fifth-order modulator shown in Figure 4 as a function of the input signal IN. In a stabilization situation the order of the modulator is lowered to three, and the delay of the delay means 44 is three clock cycles. As compared with Figure 6, the output is dependent on the input signal in a desired manner. In other words, the output of the digital filter obtains values which, though they have a lower resolution, are proportionate to the input signal IN even at input signal values exceeding the point A.

The figures and the description related to them are only intended to illustrate the present invention. In their details, the method and arrangement according to the invention may vary within the scope of the attached claims.

Claims

1. A modulator, comprising at least two integrators (H1-Hn) coupled together in series and arranged to receive an input signal (IN) characterised by means for lowering the order of the modulator when the amplitude of the input signal exceeds the range at which the modulator will operate stably.

2. A modulator according to claim 2 wherein the first one, two or three integrators (H1-H3) of the at least two integrators forms a low-order modulator arrangement and the lowering means comprises means (31) for resetting all integrators subsequently coupled to the low-order modulator arrangement when the output voltage of the low-order modulator arrangement is above a pre-determined value such that the high-order modulator operates as a low order modulator.

3. A modulator according to claim 1 further comprising a quantizing means (22) coupled to the output of the last integrator (Hn) and wherein the first one, two or three integrators (H1-H3) form a low order modulator arrangement and the lowering means comprises coupling means (MUX) for decoupling the output of-the last integrator from the quantizing means and for coupling the output voltage from the low-order modulator arrangement to the quantizing means when the output voltage from the last integrator exceeds a predetermined value, such that the high-order modulator operates as a low-order modulator.

4. A modulator according to claim 3 wherein the lowering means further comprises means (42) for resetting all integrators subsequently coupled to the low-order modulator arrangement when the output voltage from the last integrator exceeds a predetermined value.

5. A modulator according to claim 3 or claim 4 wherein the coupling means is operable to recouple the output of the last integrator stage to the quantizing means after the voltage of the last integrator falls below the predetermined value.

6. A modulator according to claim 5 wherein the coupling means is operable to recouple the output of the last integrator to the quantizing means after a predetermined delay.

7. A modulator according to claim 6 wherein the predetermined delay is at least one clock cycle for each integrator coupled subsequent to the low order modulator.

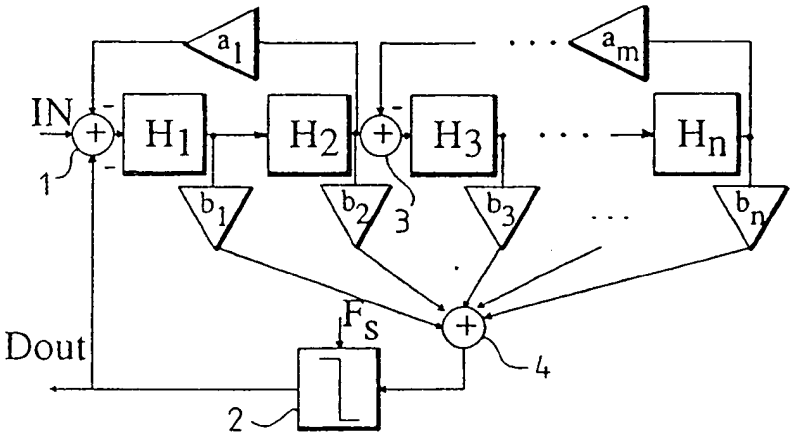


FIG. 1

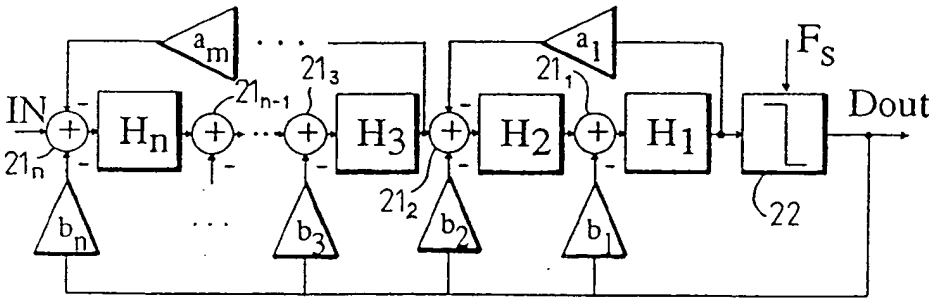


FIG. 2

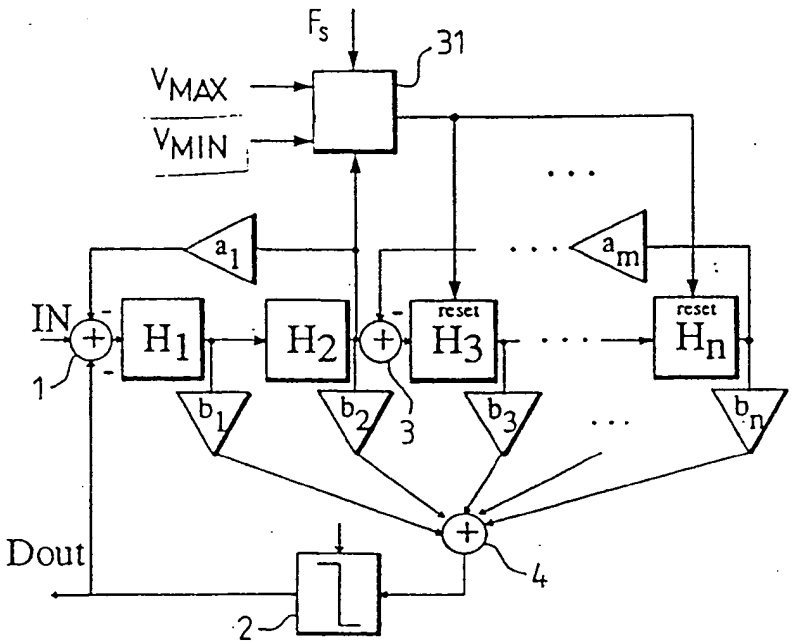


FIG. 3

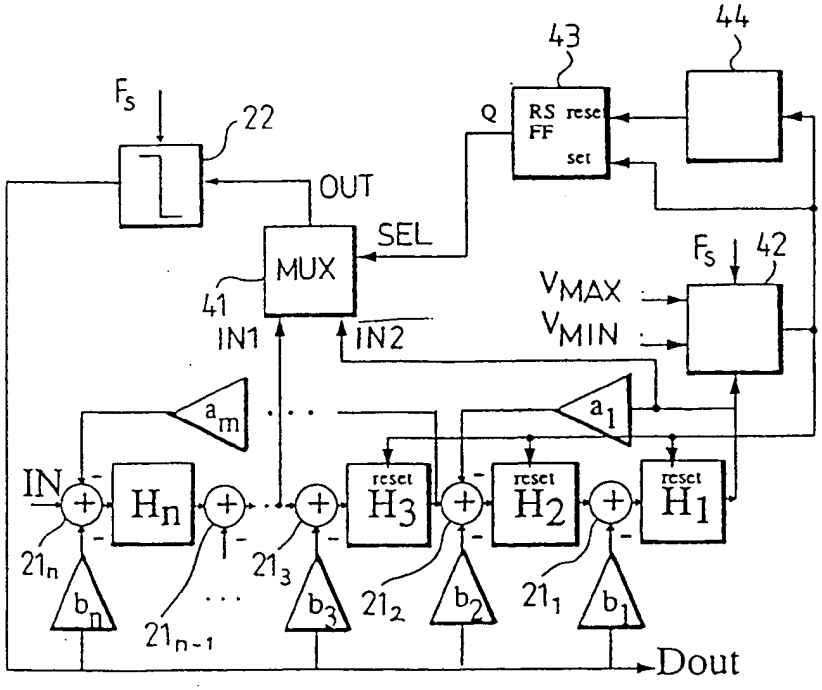


FIG. 4

FIG. 5

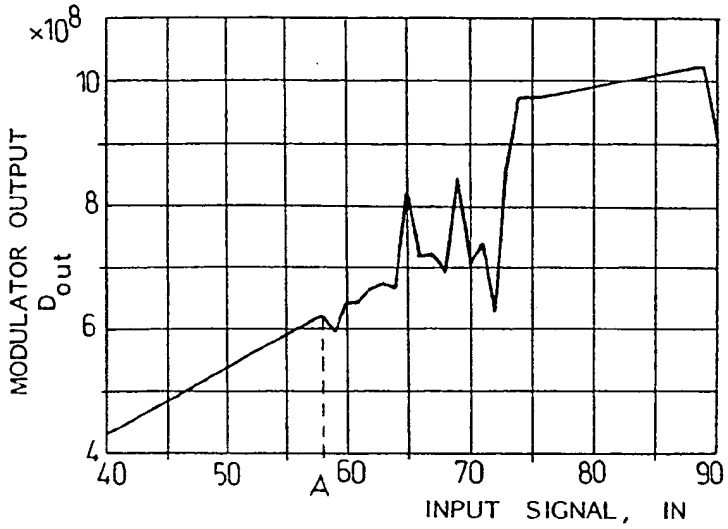


FIG. 6

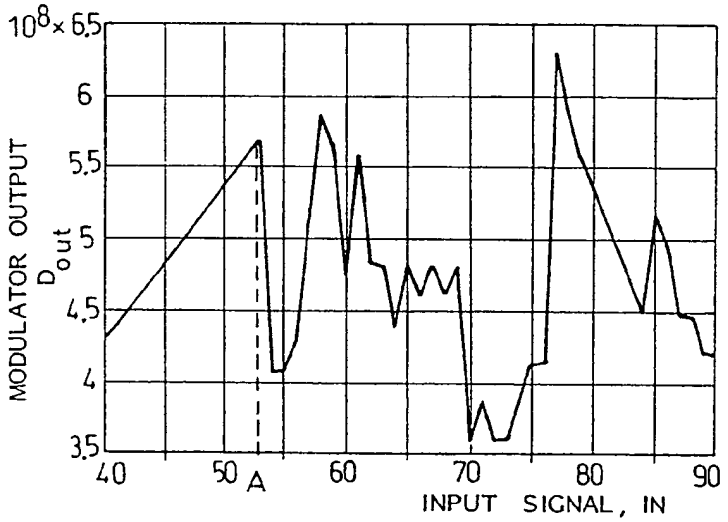
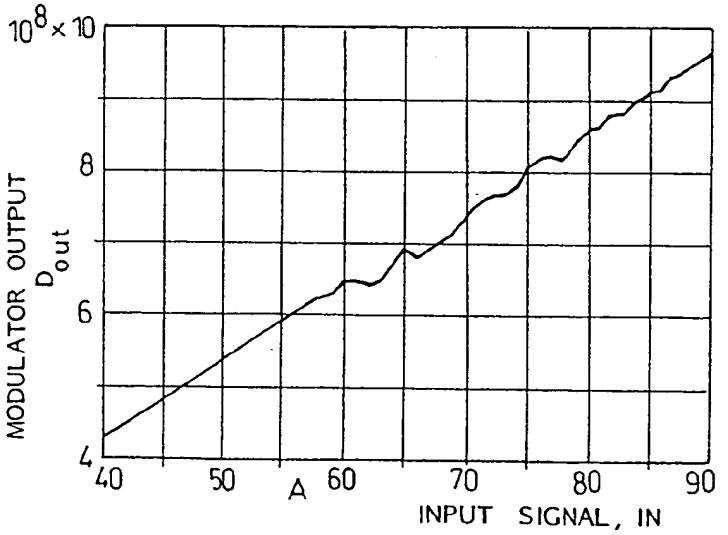


FIG. 7



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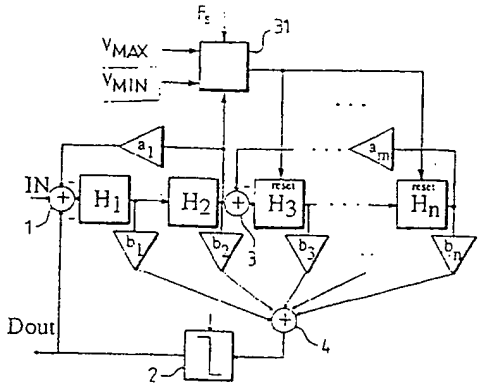

FIG. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 92 30 3093

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	US-A-5 012 244 (D. WELLARD ET AL.) * abstract; figure 2 * * column 2, line 22 - line 65 * * column 4, line 22 - column 6, line 5 *	1-4	H03M3/02
E	EP-A-0 501 580 (PHILIPS) * abstract; claim 1; figures 1,2 * * column 2, line 53 - column 4, line 13 * * column 4, line 28 - column 6, line 11 *	1	
A	WO-A-8 204 508 (GOULD) * abstract; figure 2 * * page 18, line 8 - page 20, line 18 *	1	
A	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS vol. 37, no. 3, March 1990, NEW YORK US pages 309 - 318 K. CHAO ET AL. 'A Higher Order Topology for Interpolative Modulators for Oversampling A/D Converters' * page 311, left column, paragraph 2 - page 313, left column, paragraph 2 *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE vol. 34, February 1991, NEW YORK US pages 62 - 63 F. EYNDE ET AL. 'A CMOS Fourth-Order 14b 500k-Sample/s Sigma-Delta ADC Converter' * the whole document *	1	H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	29 MARCH 1993	SAAM C.

CATEGORY OF CITED DOCUMENTS

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